AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer overlaid by a single barrier layer overlaid by a single etch stop layer overlaid by a first layer,

wherein the D-mode and E-mode FETs each include a source contact, a drain contact, and a gate contact, and

wherein the respective source and drain contacts of the D-mode FET and E-mode FET are coupled to the first layer, and the respective gate contacts of the D-mode FET and E-mode FET are coupled to the single barrier layer.

2. (Original) The integrated circuit of claim 1, further comprising a solid state amorphization region beneath the E-mode gate contact at least within the barrier layer.

3. (Original) The integrated circuit of claim 2, wherein the solid state amorphization region includes at least one compound including at least one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

4. (Original) The integrated circuit of claim 2, wherein the solid state amorphization region includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and

rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

5. (Original) The integrated circuit of claim 2, wherein the multi-layer structure further comprises at least an epitaxial second layer between the barrier layer and the first layer.

6. (Original) The integrated circuit of claim 2, wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the solid state amorphization region is within the implant region.

7. (Currently Amended) An integrated circuit comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer overlaid by a single barrier layer overlaid by a single etch stop layer overlaid by a first layer overlaid by a second layer adjacent to the first layer,

wherein the D-mode and E-mode FETs each include a source contact, a drain contact, and a gate contact,

wherein the source and drain contacts of the D-mode FET and the E-mode FET are coupled to the second layer,

wherein the gate contact of the D-mode FET is coupled to the first layer, and a solid state amorphization region is beneath the D-mode gate contact within the first layer, and

wherein the gate contact of the E-mode FET is coupled to the single barrier layer, and a solid state amorphization region is beneath the E-mode gate contact within the single barrier layer.

8. (Currently Amended) The integrated circuit of claim 7, wherein the ~~multi-layer substrate structure includes an epitaxial third layer between the first layer and the barrier layer, said third layer having~~ etch stop layer has a different composition than the first layer and the barrier layer, and wherein the D-mode solid state amorphization region is within the ~~third~~ etch stop layer.

9. (Original) The integrated circuit of claim 7, wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the E-mode solid state amorphization region is within the implant region.

10. (Original) The integrated circuit of claim 7, wherein the D-mode and E-mode solid state amorphization regions include at least one compound including platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

11. (Original) The integrated circuit of claim 7, wherein the at least one of the D-mode and E-mode solid state amorphization regions includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium, and at least one of the compounds

includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium.

12. (Currently Amended) An integrated circuit comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer overlaid by a single barrier layer overlaid by a single etch stop layer overlaid by at least by a first layer;

wherein the D-mode and E-mode FETs each include a source contact, a drain contact, and a gate contact,

wherein the source and drain contacts of the D-mode FET and the E-mode FET are coupled to one of the epitaxial layers overlying the channel layer,

wherein a gate contact of the D-mode FET is coupled to one of the first layer and the single barrier layer,

wherein a gate contact of the E-mode FET is coupled to one of the first layer and the single barrier layer, and

wherein a solid state amorphization region is present beneath the E-mode gate contact at least within the single barrier layer.

13. (Original) The integrated circuit of claim 12, wherein the D-mode gate contact is coupled to the first layer, and the E-mode gate contact is coupled to the barrier layer.

14. (Original) The integrated circuit of claim 13, further comprising a second solid state amorphization region disposed beneath the D-mode gate contact at least within the first layer.

15. (Original) The integrated circuit of claim 12, wherein the D-mode and E-mode source and drain contacts are coupled to the first layer, and the D-mode and E-mode gate contacts are coupled to the barrier layer.

16. (Original) The integrated circuit of claim 12, wherein the D-mode and E-mode source and drain contacts are coupled to the first layer, and the E-mode gate contact is coupled to the barrier layer.

17. (Original) The integrated circuit of claim 12, wherein the barrier layer is of a first conductivity type; and

further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact,

wherein the E-mode solid state amorphization region is within the implant region.

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (New) An integrated circuit comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer overlaid by a single barrier layer overlaid by a single etch stop layer overlaid by a first layer,

wherein the D-mode and E-mode FETs each include a source contact, a drain contact, and a gate contact, and

wherein the respective source and drain contacts of the D-mode FET and E-mode FET are coupled to the first layer, the gate contact of the E-mode FET is coupled to the single barrier layer and the gate contact of the D-mode FET is coupled to the single etch stop layer.

29. (New) The integrated circuit of claim 28, further comprising a solid state amorphization region beneath the E-mode gate contact at least within the barrier layer.

30. (New) The integrated circuit of claim 29, wherein the solid state amorphization region includes at least one compound including at least one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

31. (New) The integrated circuit of claim 29, wherein the solid state amorphization region includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

32. (New) The integrated circuit of claim 29, wherein the multi-layer structure further comprises at least an epitaxial second layer between the barrier layer and the first layer.

33. (New) The integrated circuit of claim 29, wherein the barrier layer is of a first conductivity type; and further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact, wherein the solid state amorphization region is within the implant region.